CLAIMS

What is claimed is:

1. A method comprising:

frequency dividing a high-frequency clock signal into a divided frequency; and

further dividing said divided frequency into another divided frequency in accordance with a data input (DIN).

2. The method according to claim 1 wherein said further dividing comprises dividing with a multi-bit counter adapted to receive said DIN and to further divide said clock signal in accordance with said DIN.

3. The method according to claim 2 and further comprising controlling at least one of said frequency dividing and said further dividing.

4. The method according to claim 3 wherein said controlling comprises:

passing said high-frequency clock signal through a pass gate; and

sampling said high-frequency clock signal.

5. The method according to claim 4 wherein said controlling further comprises, after said sampling, closing said pass gate at least once in a cycle associated with said high-frequency clock signal in accordance with a count value of said data input.

6. The method according to claim 4 wherein said closing comprises closing said pass gate if said count value is odd.

7. The method according to claim 3 wherein said controlling comprises controlling at least one of said high-frequency clock signal and said data input with a flip-flop (FF).

8. The method according to claim 1 wherein said frequency dividing comprises dividing with a frequency divider that comprises a D-type flip-flop (D-FF) that feeds its Q-bar output into its data input.

9. Apparatus comprising:

a frequency divider adapted to divide a high-frequency clock signal into a divided frequency; and

a multi-bit counter adapted to receive an output from said frequency divider and to further divide said clock signal in accordance with a data input (DIN).

10. Apparatus according to claim 9 wherein said frequency divider comprises a dual modulus frequency divider.

11. Apparatus according to claim 9 wherein said frequency divider comprises a D-type flip-flop (D-FF) that feeds its Q-bar output into its data input.

12. Apparatus according to claim 9 wherein said multi-bit counter comprises a 2n-bit counter adapted to receive data inputs DIN<1:(2^n-1)>.

13. Apparatus according to claim 9 and further comprising control logic circuitry adapted to control a count precision of said multi-bit counter.

14. Apparatus according to claim 13 wherein said control logic circuitry comprises a flip flop.

15. Apparatus comprising:

a frequency divider adapted to divide a high-frequency clock signal into a divided frequency;

a multi-bit counter adapted to receive an output from said frequency divider and to further divide said clock signal in accordance with a data input (DIN); and

an integrated circuit.

16. Apparatus according to claim 15 wherein said frequency divider comprises a dual modulus frequency divider.